**Amendments to the Specification:**

Please replace the paragraph [0004] with the following rewritten paragraph [0004]:

**[0004]** ECC's may detect single- and multi-bit errors in a data stream. Single-bit errors are most often caused by a random transient event. ECC's also have the ability to correct most single-bit errors, allowing the system to operate without downtime attributable to correctable single-bit errors. However, there are certain types of single-bit errors that are uncorrectable. These uncorrectable single-bit errors are sometimes referred to as "sticky bits." A "sticky bit" usually is the result of a physical problem in the memory device. A "sticky bit" does not always change~~s~~ state when requested. In addition, there are multi-bit errors that are typically uncorrectable. The multi-bit errors may be the result of a physical problem in the memory device, like a "sticky bit," or they may be the result of some other random transient event.

Please replace the paragraph [0006] with the following rewritten paragraph [0006]:

**[0006]** ~~In order to~~ To improve the reliability and availability of ~~a~~ such a system, what is needed is a solution that may, upon identification of an uncorrectable error, switch to a redundant backup memory system so that the system may continue operating without downtime. In addition, what is needed is a solution that is able to test the memory device to determine if the uncorrectable error is due to a physical problem with the memory device, or due to a random transient event.

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